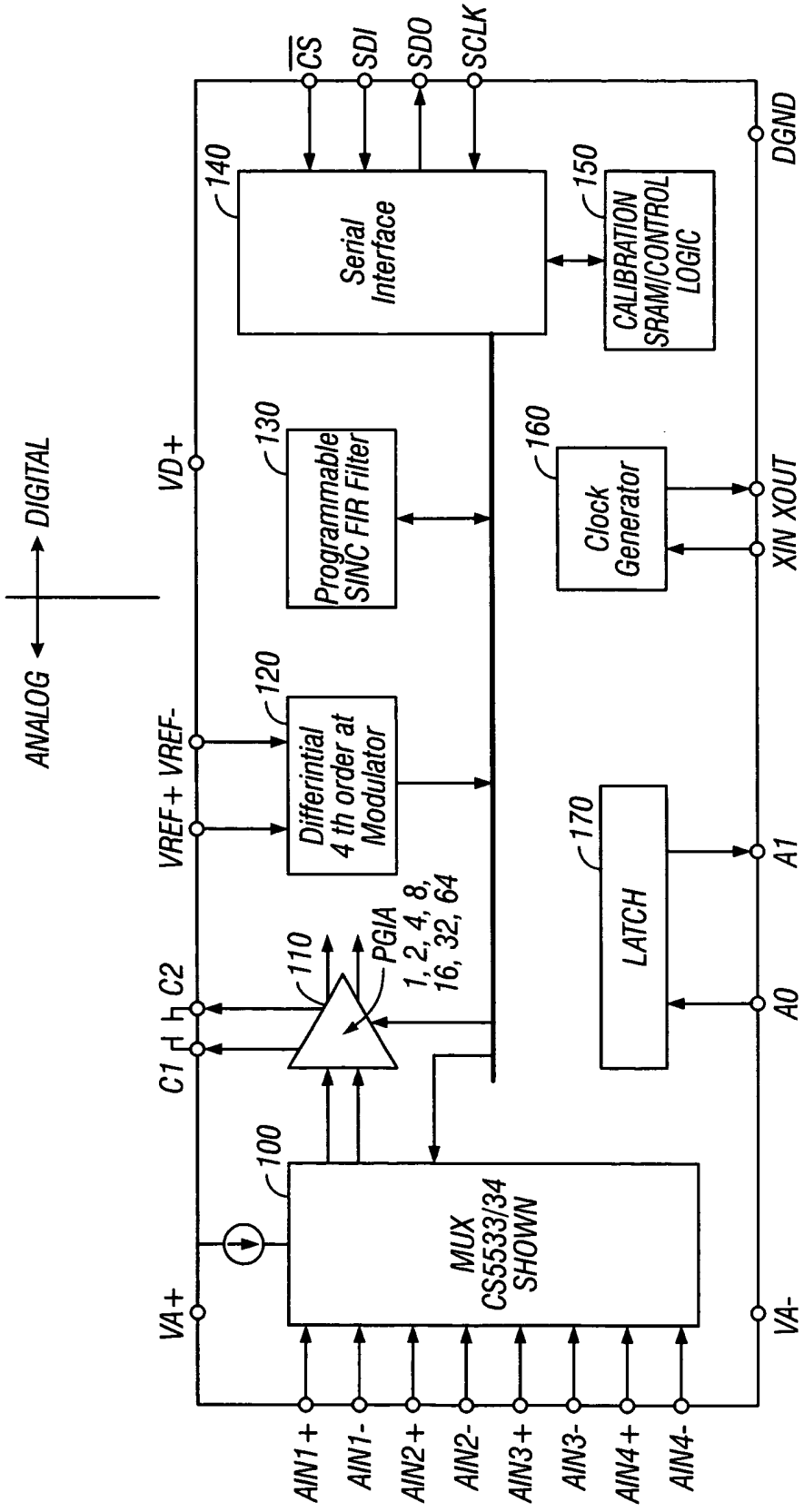
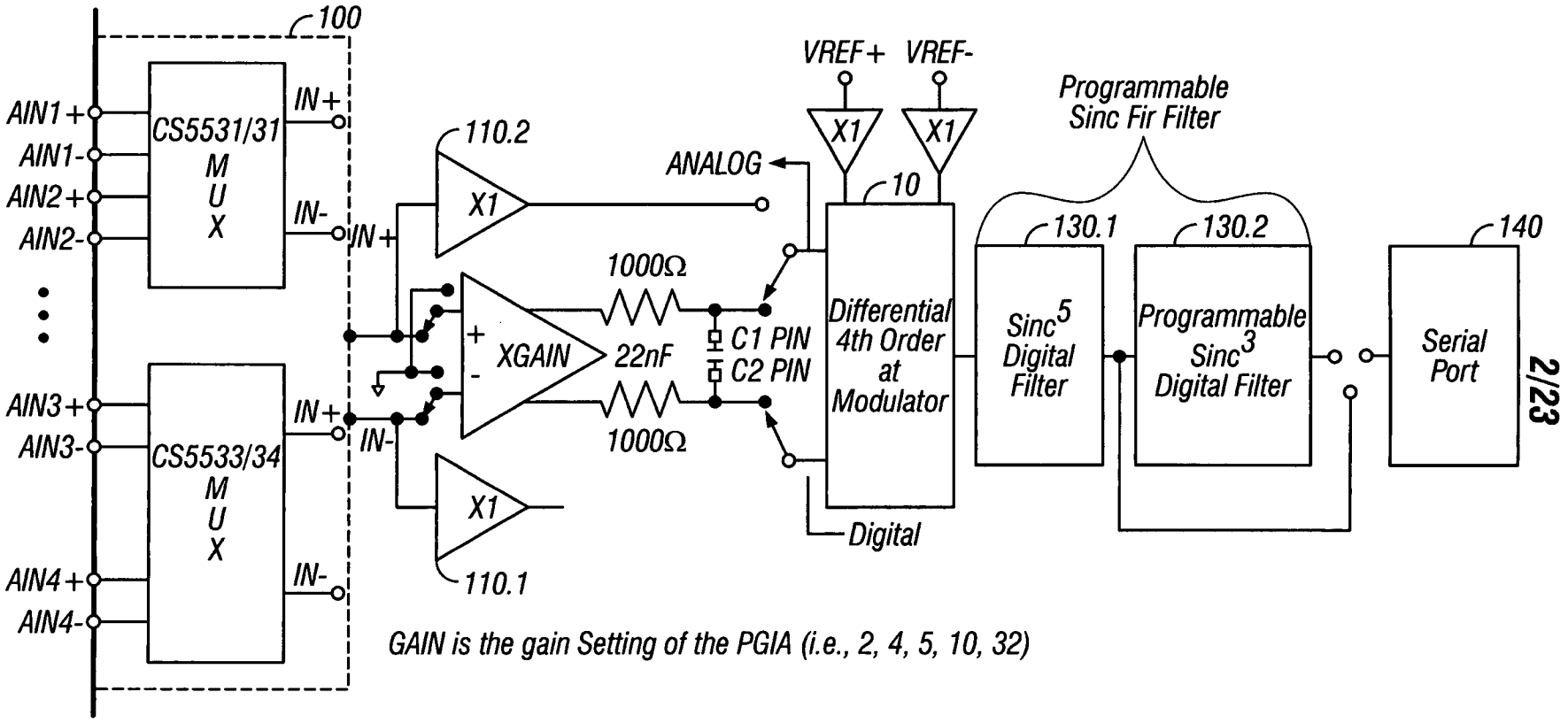


FIG. 1.A



GAIN is the gain Setting of the PGIA (i.e., 2, 4, 5, 10, 32)

FIG. 1.2

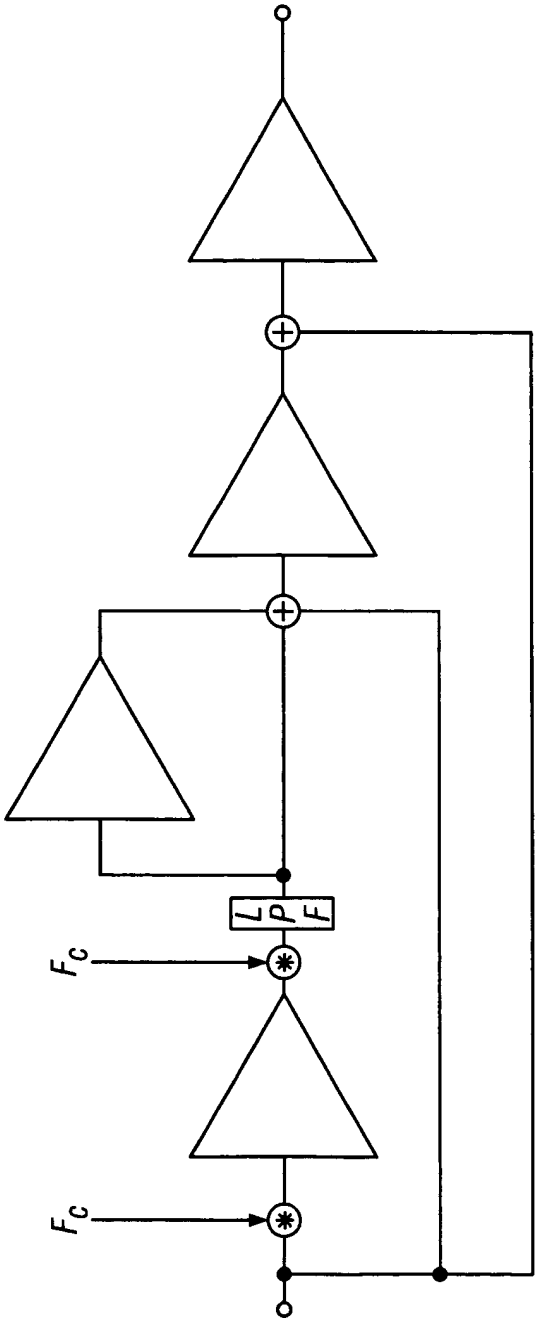


FIG. 1.3

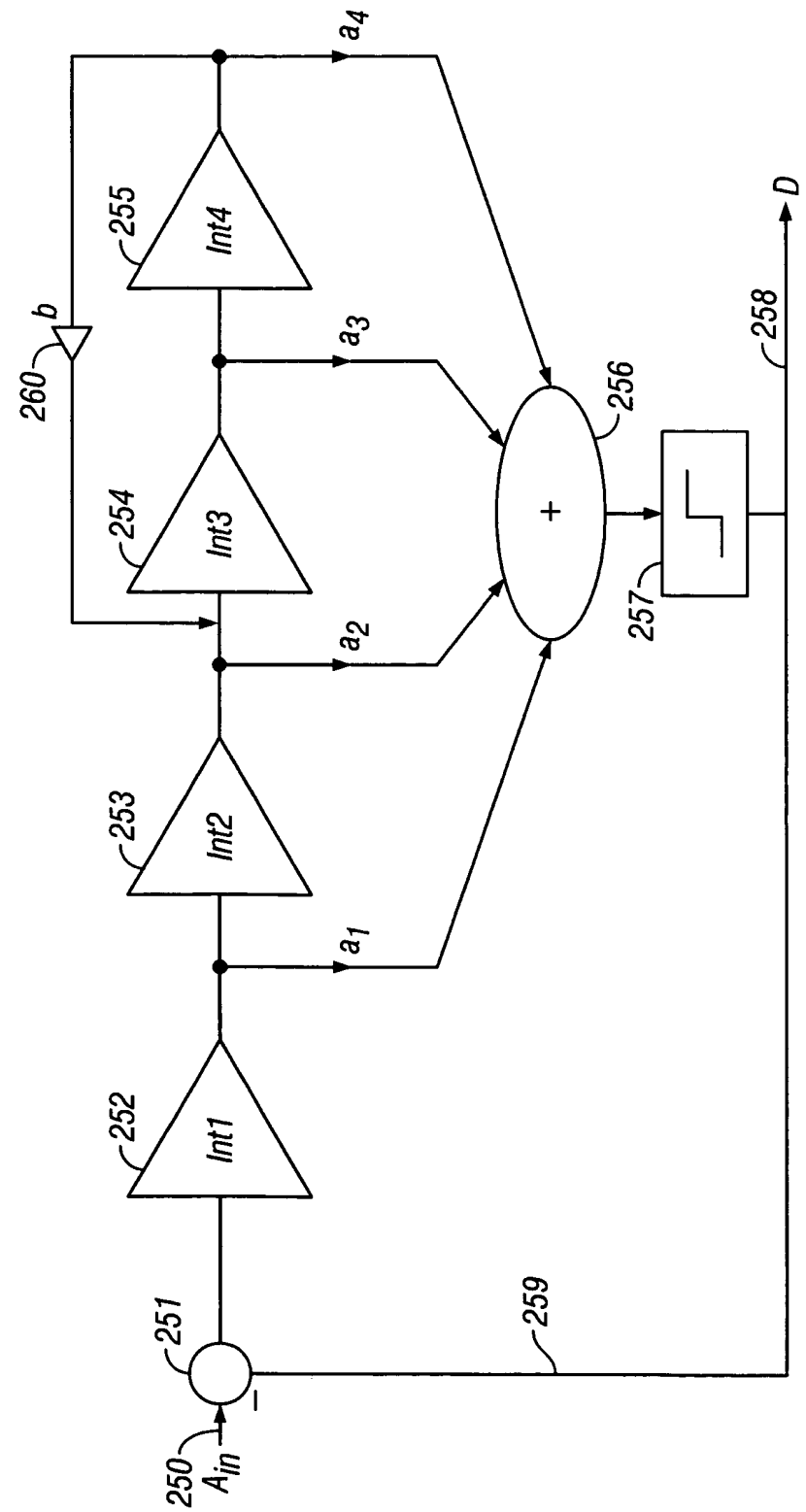


FIG. 1.4

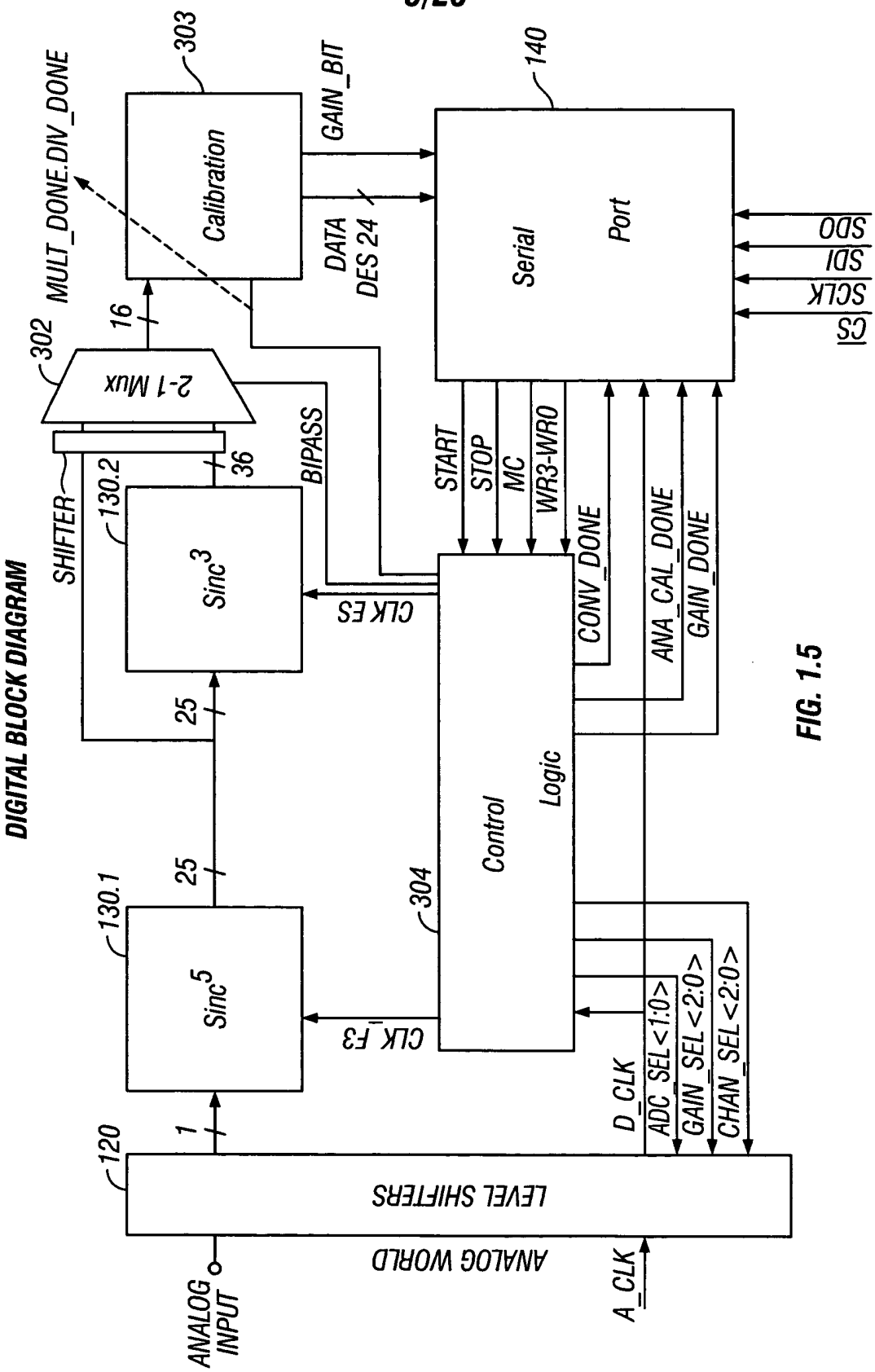

DIGITAL BLOCK DIAGRAM
303
Calibration
MULT_DONE.DIV_DONE
GAIN_BIT
DATA
DES 24
140
Serial
Port
SDO
SDI
SCLK
CS
302
2-1 Mux
16
SHIFTER
130.2
Sinc3
36
BIPASS
START
STOP
MC
WR3-WR0
CONV_DONE
ANA_CAL_DONE
GAIN_DONE
CLK_ES
25
130.1
Sinc5
25
304
Control
Logic
CLK_F3
D_CLK
ADC_SEL<1:0>
GAIN_SEL<2:0>
CHAN_SEL<2:0>
120
1
LEVEL SHIFTERS
ANALOG WORLD
ANALOG INPUT
A_CLK

FIG. 1.5

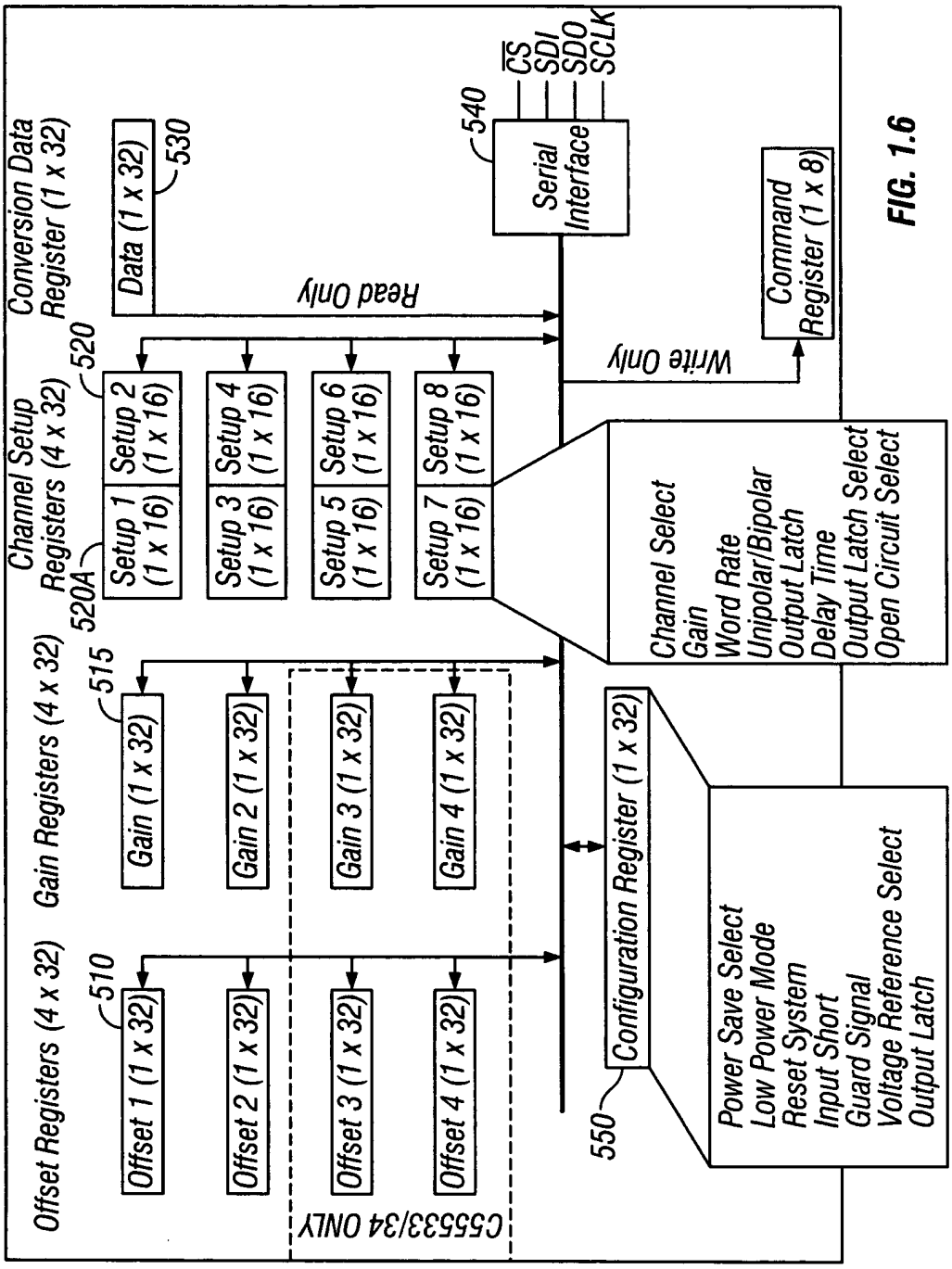

Offset Registers (4 x 32)
Gain Registers (4 x 32)
Channel Setup Registers (4 x 32)
Conversion Data Register (1 x 32)
Offset 1 (1 x 32)
Offset 2 (1 x 32)
Offset 3 (1 x 32)
Offset 4 (1 x 32)
Gain (1 x 32)
Gain 2 (1 x 32)
Gain 3 (1 x 32)
Gain 4 (1 x 32)
Setup 1 (1 x 16)
Setup 2 (1 x 16)
Setup 3 (1 x 16)
Setup 4 (1 x 16)
Setup 5 (1 x 16)
Setup 6 (1 x 16)
Setup 7 (1 x 16)
Setup 8 (1 x 16)
Data (1 x 32)
Read Only
Write Only
Serial Interface
CS
SDI
SDO
SCLK
Command Register (1 x 8)
Channel Select
Gain
Word Rate
Unipolar/Bipolar
Output Latch
Delay Time
Output Latch Select
Open Circuit Select
Configuration Register (1 x 32)
Power Save Select
Low Power Mode
Reset System
Input Short
Guard Signal
Voltage Reference Select
Output Latch
C5533/34 ONLY
510
515
520
520A
530
540
550

FIG. 1.6

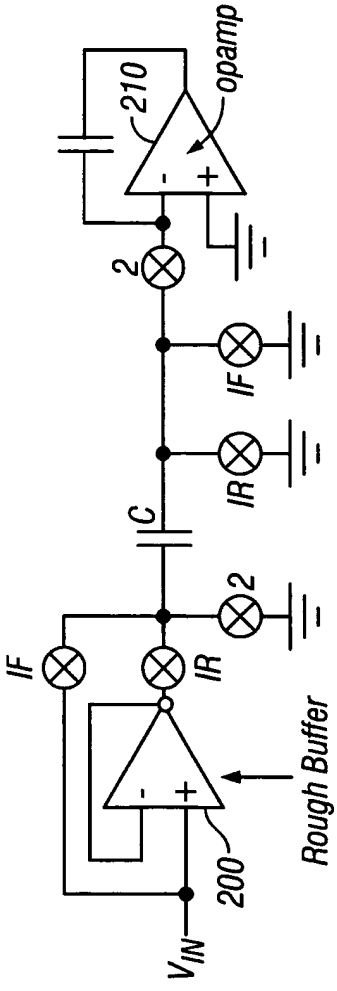

opamp
210
2
IF
IR
C
IR
IF
2
IF
IR
Rough Buffer
200
V_{IN}

FIG. 2.0

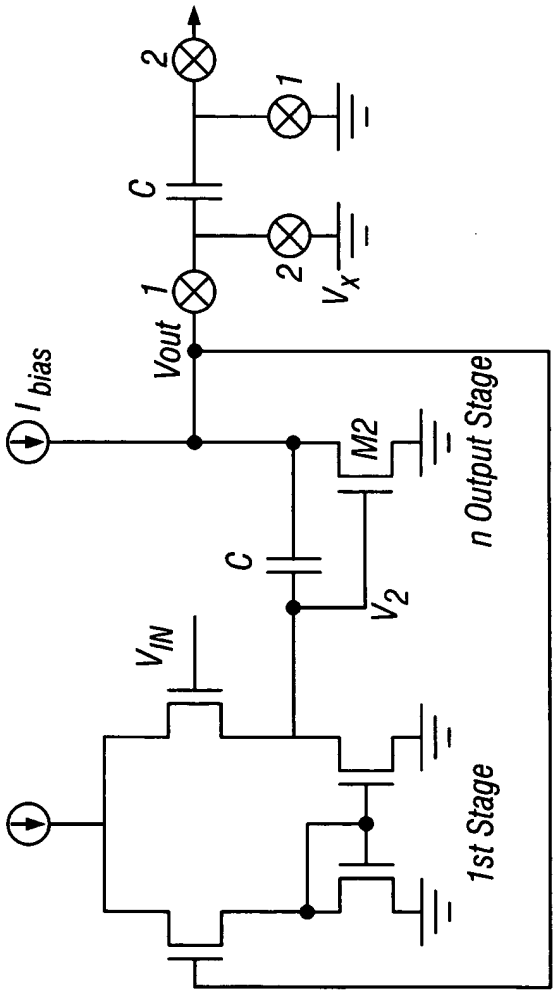

2
1
C
2
V_x
Vout 1
I_{bias}
M2
C
V_2
V_{IN}
n Output Stage
1st Stage

FIG. 2.1

V_{IN} = CONSTANT

$V_{OUT} > V_x$

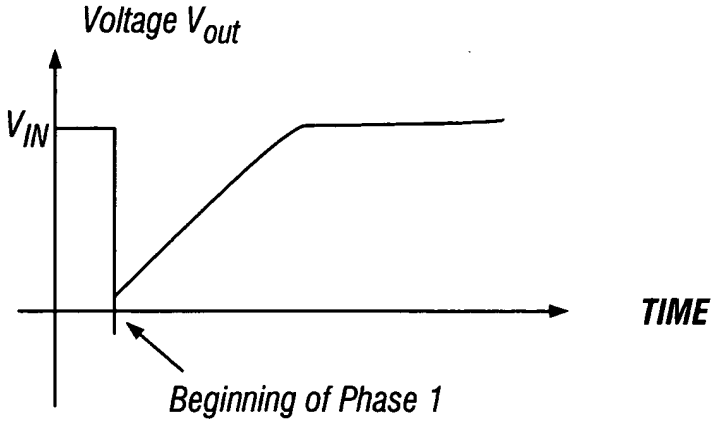


FIG. 2.2

V_{IN} = CONSTANT

$V_{OUT} < V_x$

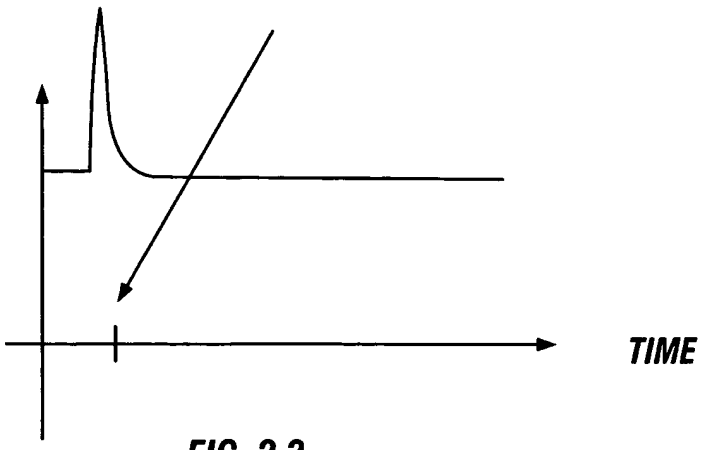


FIG. 2.3

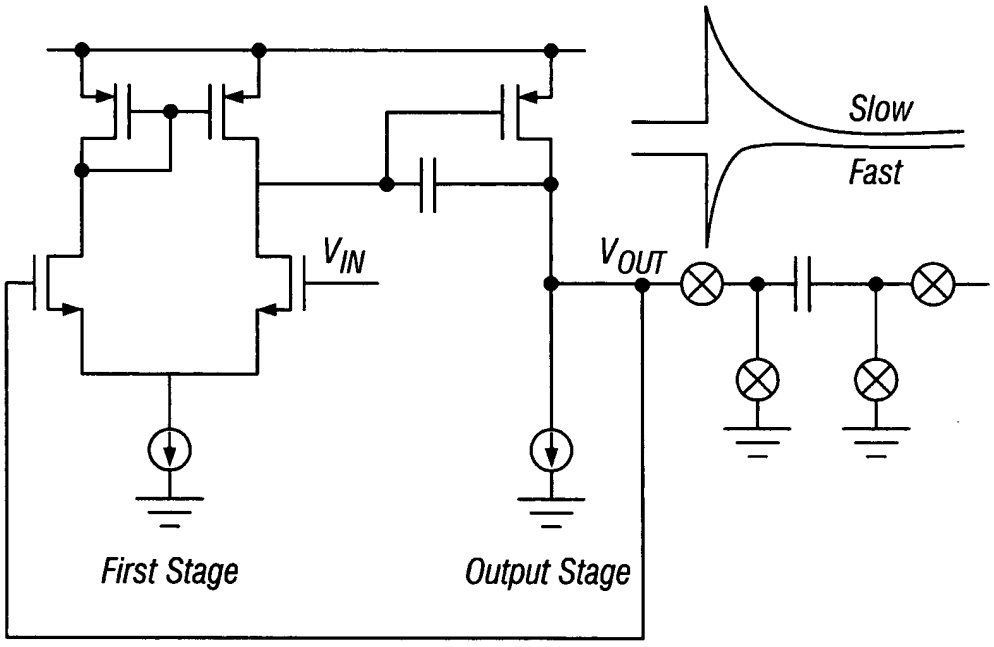


FIG. 2.4

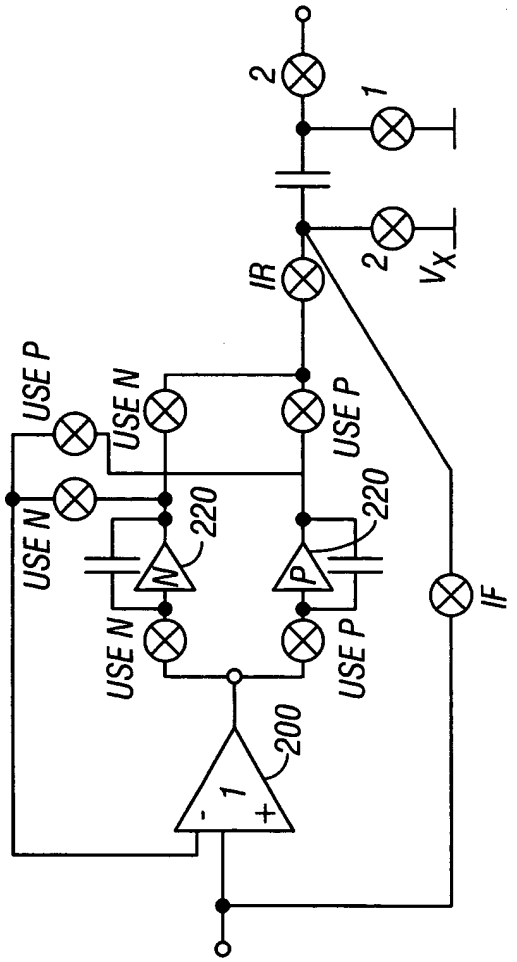
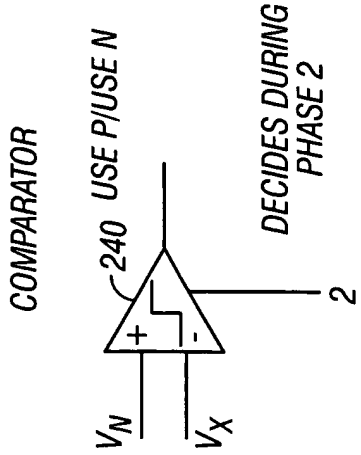

2
1
2
V_X
IR
USE P
USE N
USE P
USE N
220
220
N
P
USE N
USE P
IF
200
1
-
+

FIG. 2.5


COMPARATOR
USE P/USE N
240
DECIDES DURING PHASE 2
2
+
-
V_N
V_X

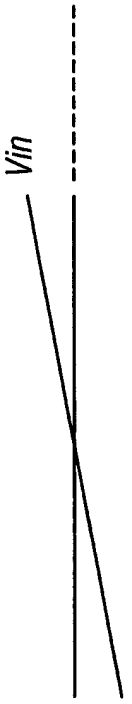


FIG. 2.6

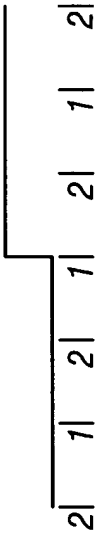


FIG. 2.7

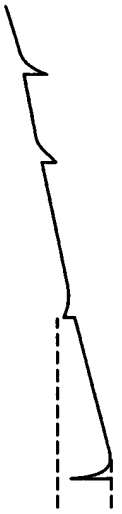


FIG. 2.8

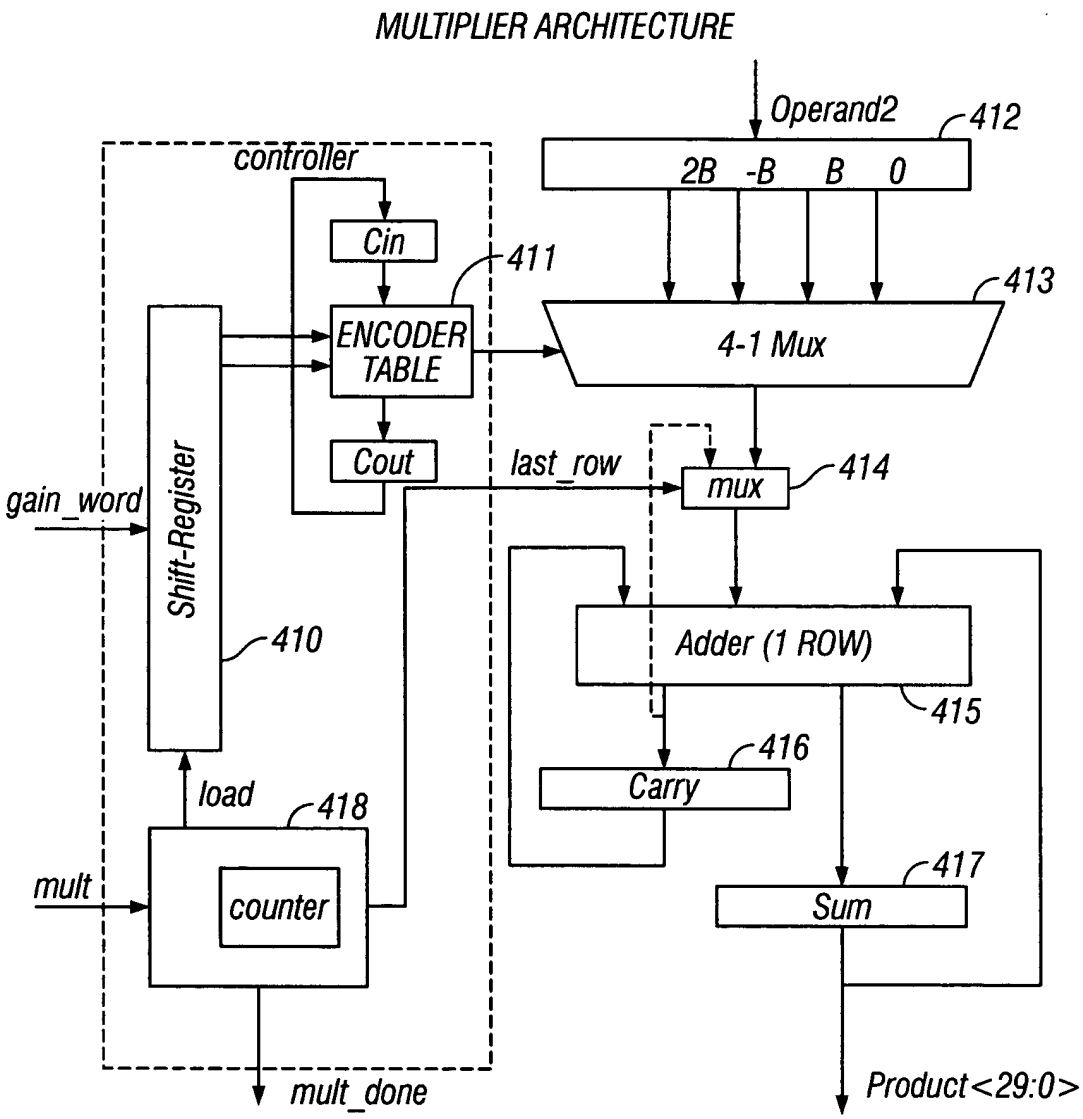

MULTIPLIER ARCHITECTURE
Operand2
412
2B -B B 0
controller
Cin
411
413
ENCODER TABLE
4-1 Mux
Cout
last_row
mux
414
gain_word
Shift-Register
410
Adder (1 ROW)
415
416
Carry
load
418
mult
counter
417
Sum
mult_done
Product<29:0>

FIG. 3.1

A_{i+1}	A_1	Operation
0	0	$R_i=R_{i-1}/4$
0	1	$R_i=(R_{i-1}+B)/4$
1	0	$R_i=(R_{i-1}+2B)/4$
1	1	$R_i=(R_{i-2}+3B)/4$

FIG. 3.2
(Prior Art)

Cin	A_{i+1}	A_i	Operation	Cout
0	0	0	$R_i=R_{i-1}/4$	0
0	0	1	$R_i=(R_{i-1}+B)/4$	0
0	1	0	$R_i=(R_{i-1}+2B)/4$	0
0	1	1	$R_i=(R_{i-2}-3B)/4$	1
1	0	0	$R_i=(R_{i-1}+B)/4$	0
1	0	1	$R_i=(R_{i-1}+2B)/4$	0
1	1	0	$R_i=(R_{i-1}-B)/4$	0
1	1	1	$R_i=(R_{i-1})/4$	1

FIG. 3.3
(Prior Art)

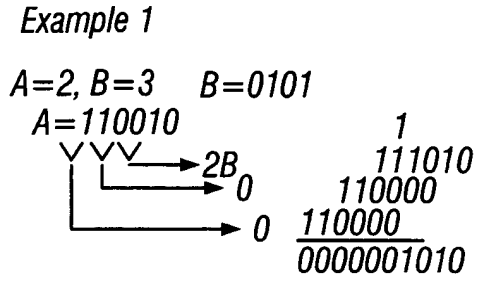

Example 1
A=2, B=3 B=0101
A=110010
2B
0
0
1
111010
110000
110000
0000001010

FIG. 3.4

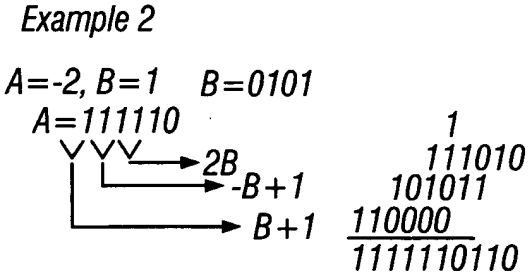

Example 2
A=-2, B=1 B=0101
A=111110
2B
-B+1
B+1
1
111010
101011
110000
1111110110

FIG. 3.5

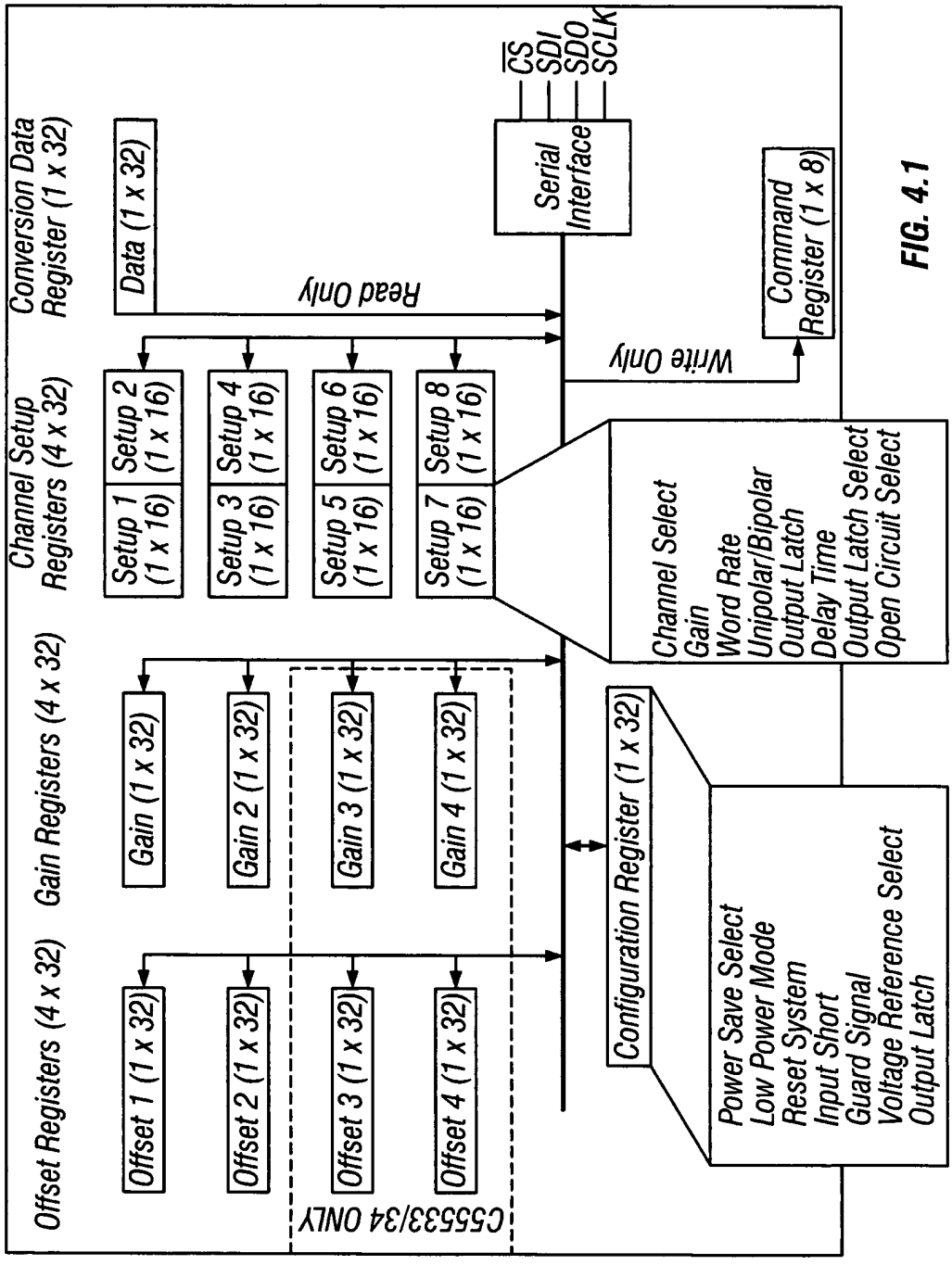

Offset Registers (4 x 32)
Gain Registers (4 x 32)
Channel Setup Registers (4 x 32)
Conversion Data Register (1 x 32)
Offset 1 (1 x 32)
Offset 2 (1 x 32)
Offset 3 (1 x 32)
Offset 4 (1 x 32)
Gain (1 x 32)
Gain 2 (1 x 32)
Gain 3 (1 x 32)
Gain 4 (1 x 32)
Setup 1 (1 x 16)
Setup 2 (1 x 16)
Setup 3 (1 x 16)
Setup 4 (1 x 16)
Setup 5 (1 x 16)
Setup 6 (1 x 16)
Setup 7 (1 x 16)
Setup 8 (1 x 16)
Data (1 x 32)
Read Only
Write Only
Serial Interface
CS
SDI
SDO
SCLK
Command Register (1 x 8)
Channel Select
Gain
Word Rate
Unipolar/Bipolar
Output Latch
Delay Time
Output Latch Select
Open Circuit Select
Configuration Register (1 x 32)
Power Save Select
Low Power Mode
Reset System
Input Short
Guard Signal
Voltage Reference Select
Output Latch
C5553/34 ONLY

FIG. 4.1

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	ARA	CS1	CS0	R/$\overline{W}$	RSB2	RSB1	RSB0

BIT	NAME	VALUE FUNCTION
D7	COMMAND Bit, C	0 Must be logic 0 for these commands. 1 These commands are invalid if this bit is logic 1.
D6	Access Registers as Arrays, ARA	0 Ignore this function. 1 Access the respective registers, offset, gain, or channel-setup, as an array registers. The particular registers accessed are determined by the RS bits. The register are accessed MSB first with physical channel 0 accessed first followed by physical channel 1 next and so forth.
D5-D4	Channel Select Bits, CS1-CS0)	00 CS1-CS0 provide the address of one of the two (four for CS5533/34) physical input 01 channels. These bits are also used to access the calibration registers associated 10 with the respective physical input channel. Note that these bits are ignored when 11 reading data register.
D3	Read/$\overline{\text{Write}}$, R/$\overline{W}$	0 Write to selected register. 1 Read from selected register.
D2-D0	Register Select Bit, RSB3-RSB0	000 Reserved 001 Offset Register 010 Gain Register 011 Configuration Register 100 Conversion Data Register (Read Only) 101 Channel-Setup Registers 110 Reserved 111 Reserved

FIG. 4.2

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

BIT	NAME	VALUE FUNCTION
D7	COMMAND Bit, C	0 These commands are invalid if this bit is logic 0. 1 Must be logic 1 for these commands.
D6	Multiple Conversions, MC	0 Perform fully settled single conversions. 1 Perform conversions continuously.
D5-D3	Channel Setup Register Pointer Bits, CSRP	000 These bits are used as pointers to the Channel-Setup registers. Either a single conversion or continuous conversions are preformed on the channel setup register ... pointed to by these bits. 111
D2-D0	Conversion/Calibration Bits, CC2-CC0	000 Normal Conversion 001 Self-Offset Calibration 010 Self-Gain Calibrationr 011 Reserved 100 Reserved 101 System-Offset Calibration 110 System-Gain Calibration 111 Reserved

FIG. 4.3

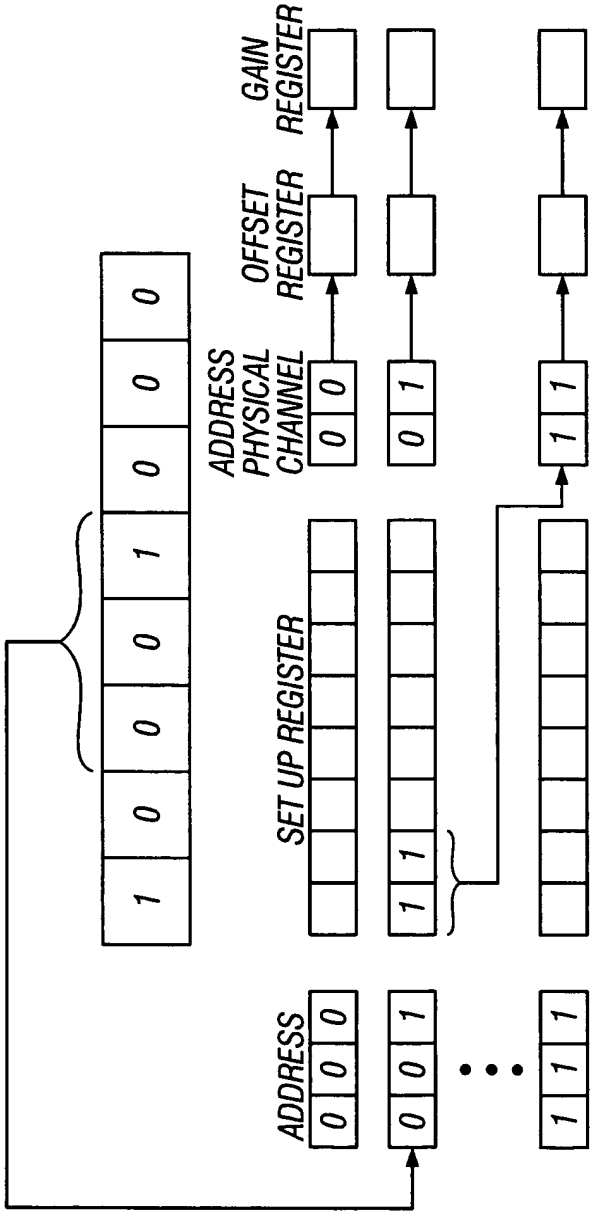

ADDRESS
0 0 0
0 0 1
1 1 1
SET UP REGISTER
1 0 0 0 1 0 0 0
1 1
ADDRESS PHYSICAL CHANNEL
0 0
0 1
1 1
OFFSET REGISTER
GAIN REGISTER

FIG. 4.4

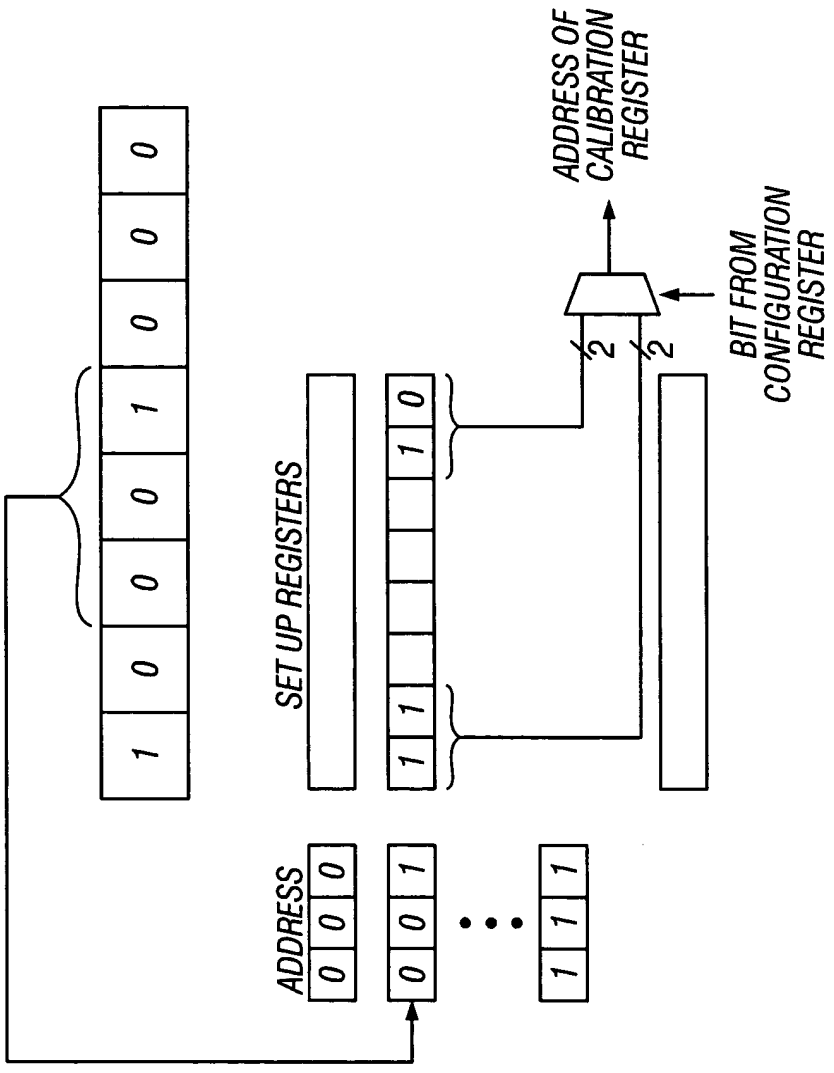

ADDRESS
0 0 0
0 0 1
1 1 1
SET UP REGISTERS
1 1
1 0
1 0 0 0 1 0 0 0
2
2
ADDRESS OF CALIBRATION REGISTER
BIT FROM CONFIGURATION REGISTER

FIG. 4.5

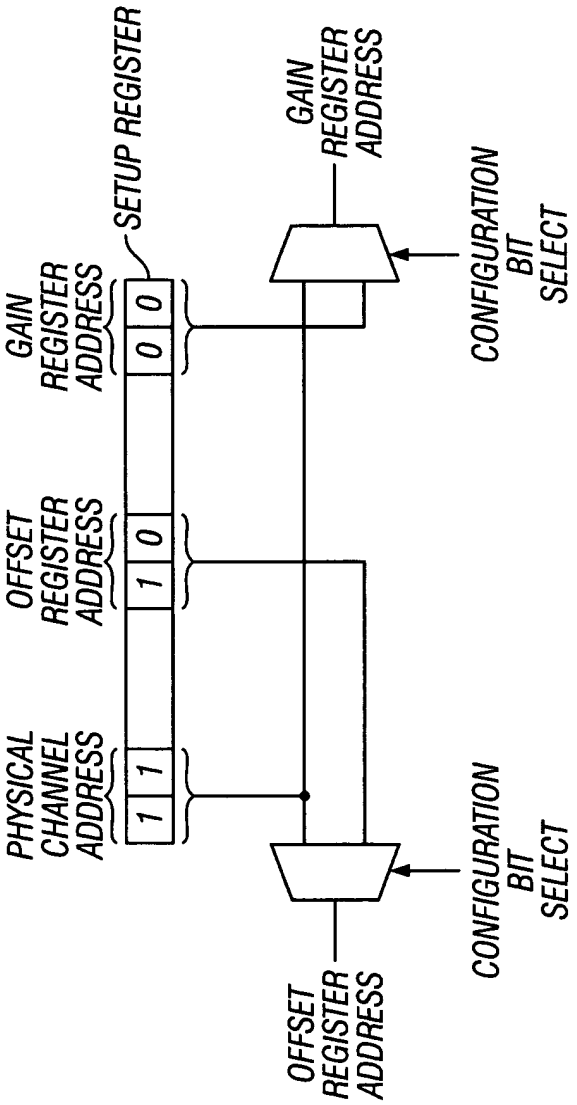

SETUP REGISTER
GAIN REGISTER ADDRESS
OFFSET REGISTER ADDRESS
PHYSICAL CHANNEL ADDRESS
1 1
1 0
0 0
GAIN REGISTER ADDRESS
CONFIGURATION BIT SELECT
CONFIGURATION BIT SELECT
OFFSET REGISTER ADDRESS

FIG. 4.6

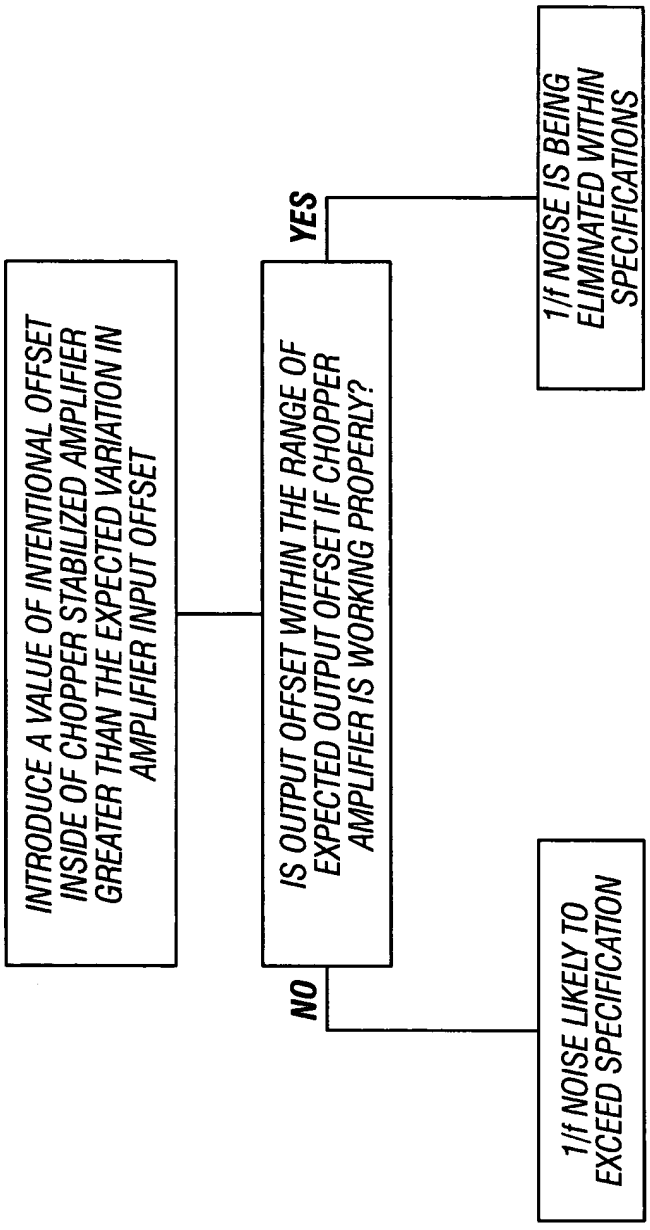

INTRODUCE A VALUE OF INTENTIONAL OFFSET INSIDE OF CHOPPER STABILIZED AMPLIFIER GREATER THAN THE EXPECTED VARIATION IN AMPLIFIER INPUT OFFSET
IS OUTPUT OFFSET WITHIN THE RANGE OF EXPECTED OUTPUT OFFSET IF CHOPPER AMPLIFIER IS WORKING PROPERLY?
YES
1/f NOISE IS BEING ELIMINATED WITHIN SPECIFICATIONS
NO
1/f NOISE LIKELY TO EXCEED SPECIFICATION

FIG. 5.1

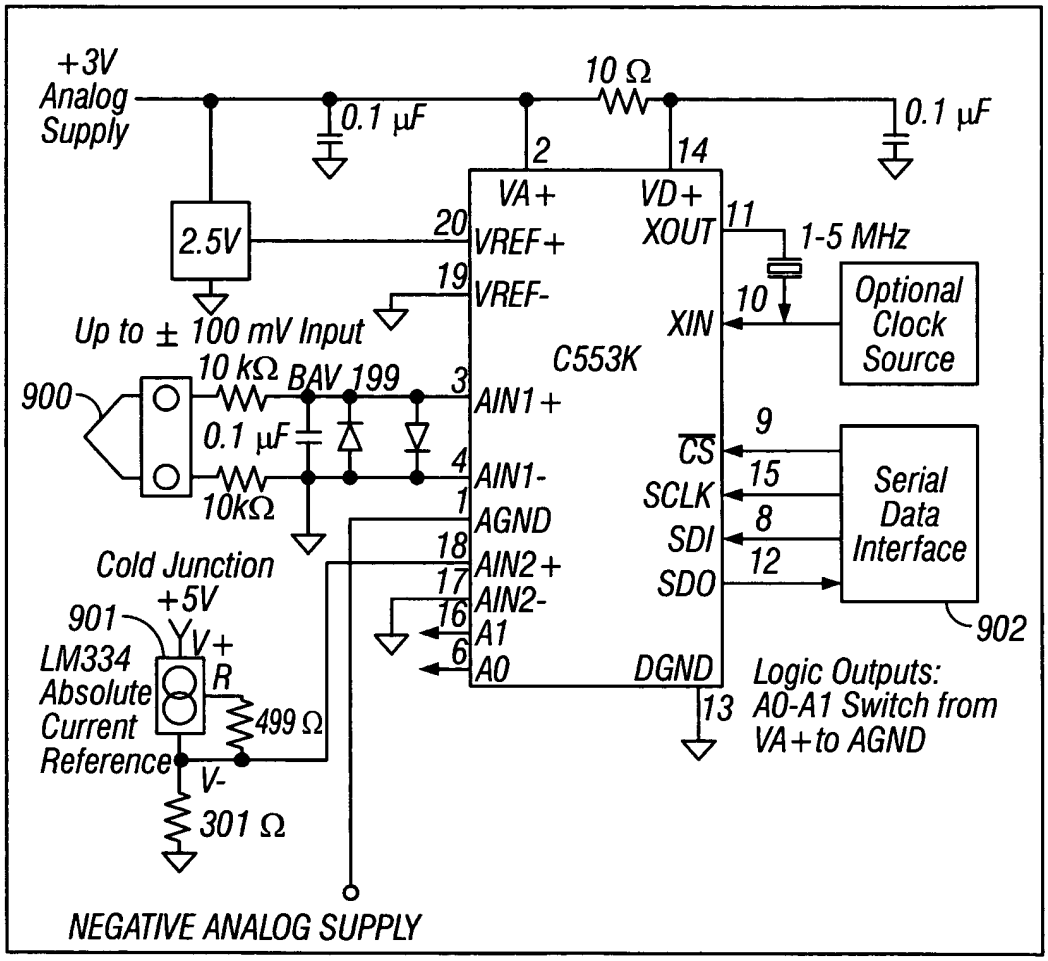

+3V
Analog
Supply
0.1 µF
10 Ω
0.1 µF
2
14
VA+
VD+
2.5V
20
VREF+
XOUT
11
1-5 MHz
19
VREF-
10
Optional
Clock
Source
Up to ± 100 mV Input
XIN
C553K
10 kΩ
BAV 199
900
3
AIN1+
9
CS
0.1 µF
4
AIN1-
15
SCLK
Serial
Data
Interface
10kΩ
1
AGND
8
SDI
Cold Junction
18
AIN2+
12
SDO
+5V
17
AIN2-
902
901
16
A1
V+
LM334
Absolute
Current
Reference
R
6
A0
DGND
Logic Outputs:
A0-A1 Switch from
VA+ to AGND
499 Ω
13
V-
301 Ω
NEGATIVE ANALOG SUPPLY

FIG. 6.1

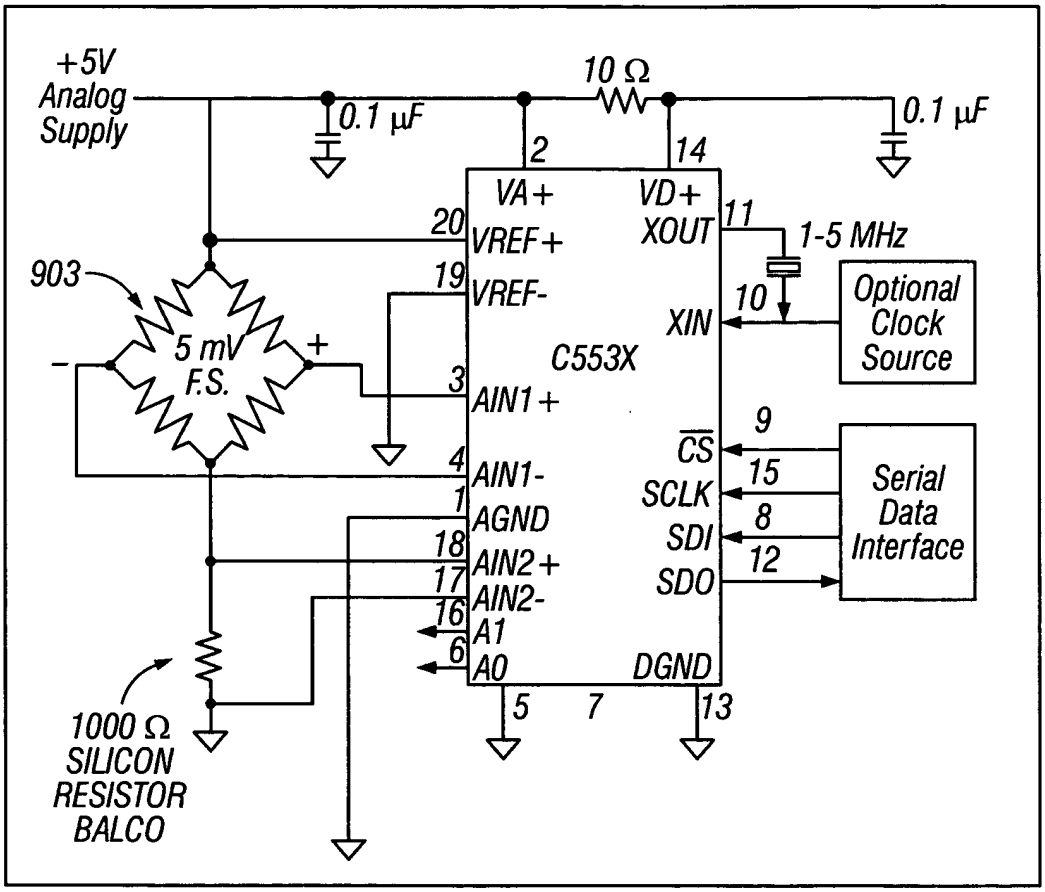

+5V
Analog
Supply
0.1 µF
10 Ω
0.1 µF
2
14
VA+
VD+
20
VREF+
XOUT
11
1-5 MHz
903
19
VREF-
10
Optional
Clock
Source
XIN
5 mV
F.S.
C553X
3
AIN1+
9
CS
4
AIN1-
15
SCLK
Serial
Data
Interface
1
AGND
8
SDI
18
AIN2+
12
SDO
17
AIN2-
16
A1
6
A0
DGND
5
7
13
1000 Ω
SILICON
RESISTOR
BALCO

FIG. 6.2